- - REMARKS - -

These remarks are in response to a Final Office Action dated August 23, 2002. Claims 1-9 are currently pending in the present application. Claims 1, 3 and 5-9 have been amended herein to particularly point out and distinctly claim the present invention in accordance with 35 U.S.C. §112, ¶2.

In the Non-Final Office Action, Examiner Meonske objected to (1) the title as not being descriptive and the abstract as being to long, and (2) the drawings for failing to comply with 37 C.R.F. §1.84(p)(5). To obviate these objections, the Applicant is concurrently filing a marked-up specification and a substitute specification in accordance with 37 CFR §1.125 as well as proposed drawing corrections of FIGS. 1 and 2. No new matter was introduced into substitute specification and the proposed drawing corrections of FIGS. 1 and 2.

Also in the Non-Final Office Action, Examiner Meonske objected to FIG. 1 because it is unclear to Examiner Meonske as to how the selectors 141-149 are duplicated as indicated by the ellipses. The Applicant respectfully asserts that the Applicant did not describe the selectors 141-149 as being identical, and that the ellipses actually indicate an omission of some of the selectors 141-149 from FIG. 1. Withdrawal of this objection to FIG. 1 is therefore respectfully requested.

Finally, in the Non-Final Office Action, Examiner Meonske rejected pending claims 1-9 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,577,189 to *Cocke* et al. The Applicant has also thoroughly read *Cocke*. To warrant this §102(b) rejection of independent claims 1, 6 and 7, *Cocke* must show each and every limitation of independent claims 1, 6 and 7 in as complete detail as in contained in independent claims 1, 6 and 7. See, MPEP §2131.

Independent Claim 1. *Cocke* discloses a BRANCH instruction for causing a processor to load an effective branch address EBA into a default-register to form the default-destination-address, and an EXIT instruction for causing the processor to subsequently execute program instructions that are located in the memory at the default-destination-address contained in the default-register. *Cocke* however fails to teach or suggest the BRANCH instruction causing the processor to concurrently execute program instructions that are located in the memory at the default-destination-address contained in the default-register as evidenced by the fact that an execution of an instruction sequence containing the BRANCH instructions is sequentially continued after an execution of the BRANCH instruction unit the EXIT instruction is reached. See, *Cocke* at column 13, line 72 to column 18, line 11.

For example, instructions OPα4- OPα7 are executed until the EXIT instruction is reached as illustrated in FIG. 5A of *Cocke*, instructions OPα2 and OPα3 are executed until the EXIT instruction is reached as illustrated in FIG. 6A of *Cocke*, and instructions OPα2, OPα3, B2 and OPα4 are executed until the EXIT instruction is reached as illustrated in FIG. 7A of *Cocke*.

The Applicant has therefore amended independent claim 1 to recite "a first instruction that is configured to cause the processor to concurrently load a specified address into the default-register to form the default-destination-address and execute program instructions that are located in the memory at the default-destination-address contained in the default-register." Withdrawal of the rejection of independent claim 1 under 35 U.S.C. §102(b) as being anticipated by *Cocke* and further examination of independent claim 1 under 37 CFR § 1.112 are therefore respectfully requested.

Claims 2-5 depend from independent claim 1. Therefore, dependent claims 2-5 include all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claims 2-5 are allowable over *Cocke* for at least the same reason as set forth with respect to independent claim 1. Withdrawal of the rejection of dependent claims 2-5 under 35 U.S.C. §102(b) as being anticipated by *Cocke* and further examination of dependent claims 2-5 under 37 CFR § 1.112 are therefore respectfully requested.

Independent Claim 6. *Cocke* discloses a BRANCH instruction for causing a processor to load result of a default-condition test into a default-register, and an EXIT instruction for causing the processor to subsequently execute program instructions that are located in the memory at a default-destination-address based on a result of the default-condition test contained in the default-register. Again, *Cocke* fails to teach or suggest the BRANCH instruction causing the processor to concurrently execute program instructions that are located in the memory at the default-destination-address contained in the default-register as evidenced by the fact that an execution of an instruction sequence containing the BRANCH instructions is sequentially continued after an execution of the BRANCH instruction unit the EXIT instruction is reached. See, *Cocke* at column 13, line 72 to column 18, line 11.

The Applicant has therefore amended independent claim 6 to recite "a first instruction that is configured to cause the processor to concurrently load a specified condition into the default-register to form the default-condition-test and execute program instructions that are located in the memory at a destination-address based on a result of the default-condition-test." Withdrawal of the rejection of independent claim 6 under 35 U.S.C. §102(b) as being anticipated by *Cocke* and further examination of independent claim 6 under 37 CFR § 1.112 are respectfully requested.

Independent Claim 7. As previously stated herein concerning independent claim 1, *Cocke* however fails to teach or suggest the BRANCH instruction causing the processor to concurrently execute program instructions that are located in the memory at the default-destination-address contained in the default-register as evidenced by the fact that an execution of an instruction sequence containing the BRANCH instructions is sequentially continued after an execution of the BRANCH instruction unit the EXIT instruction is reached. See, *Cocke* at column 13, line 72 to column 18, line 11. The Applicant has therefore amended independent claim 7 to recite "executing a first instruction that concurrently specifies a [destination-address] default-destination-address and conditionally causes the default-destination address to become a next instruction address for a first processing cycle". Withdrawal of the rejection of independent claim 7 under 35 U.S.C. §102(b) as being anticipated by *Cocke* and further examination of independent claim 7 under 37 CFR § 1.112 are respectfully requested.

Claim 8 and 9 depend from independent claim 7. Therefore, dependent claims 8 and 9 include all of the elements and limitations of independent claim 7. It is therefore respectfully submitted by the Applicant that dependent claims 8 and 9 are allowable over *Cocke* for at least the same reason as set forth with respect to independent claim 7. Withdrawal of the rejection of dependent claims 8 and 9 under 35 U.S.C. §102(b) as being anticipated by *Cocke* and further examination of dependent claims 8 and 9 under 37 CFR § 1.112 are therefore respectfully requested.

SUMMARY

Examiner Meonske's objection of the drawings and specification have been obviated by the concurrent submission of proposed drawings corrections to FIGS. 1 and 2, and the substitute specification, respectively. Examiner Meonske's 35 U.S.C. §102(b) rejection of claims 1-9 have been obviated by the amendment herein of independent claims 1, 6 and 7, and the remarks herein concerning the patentability of the amended claims 1, 6 and 7 over *Cocke*. The Applicant respectfully submits that claims 1-9 as amended herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

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Respectfully submitted,
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MARKED-UP VERSION

OF AMENDED CLAIMS TO SHOW CHANGES MADE:

1. (AMENDED) A processor that is configured to execute program instructions that are stored in a memory, said processor comprising:

a default-register that is configured to contain a default-destination-address[,]; and

wherein the program instructions include:

a first instruction that is configured to cause the processor to concurrently load a specified address into the default-register to form the default-destination-address and execute program instructions that are located in the memory at the default-destination-address contained in the default-register, and

a second instruction that is configured to cause the processor to subsequently execute the program instructions that are located in the memory at the default-destination-address contained in the default-register.

3. (AMENDED) The processor of claim 1,

wherein the default-register is further configured to contain a default-condition-test[,]; and

wherein the second instruction is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of the default-condition-test contained in the default-register.

5. (AMENDED) The processor of claim 1,

wherein the default-register is further configured to contain a default-condition-test[,]; and

wherein the program instructions further include:

a third instruction that is configured to cause the processor to execute program instructions that are located at another specified address in dependence upon a result of the default-condition-test contained in the default-register.

6. (AMENDED) A processor that is configured to execute program instructions that are stored in a memory, said processor comprising:

a default-register that is configured to contain a default-condition-test[,]; and

wherein the program instructions include:

a first instruction that is configured to cause the processor to concurrently load a specified condition into the default-register to form the default-condition-test and execute program instructions that are located in the memory at a destination-address based on a result of the default-condition-test, and

a second instruction that is configured to cause the processor to subsequently execute program instructions that are located in the memory at a destination-address[,] based on a result of the default-condition-test.

7. (AMENDED) A method of controlling a sequence of program instructions, said method comprising:

executing a first instruction that concurrently specifies a destination-address and conditionally causes the default-destination address to become a next instruction address during a first processing cycle;[,]

subsequent to an execution of the first instruction, executing a second instruction that causes the destination-address to become the next instruction address during a second processing cycle;[,] and

subsequent to an execution of the second instruction, executing a third instruction that is located at the next instruction address.

8. (AMENDED) The method of claim 7, further [including] comprising:

executing a fourth instruction, before executing the second instruction, that specifies a condition-test[,]; and

wherein causing the destination-address to become the next instruction address during the second processing cycle is dependent upon a result of the condition-test when the second instruction is executed.

9. (AMENDED) The method of claim 7, further [including] comprising:

saving a result of a condition-test, before executing the second instruction[,]; and

wherein causing destination-address to become the next instruction address during the second processing cycle when executing the second instruction is dependent upon the result of the condition-test.